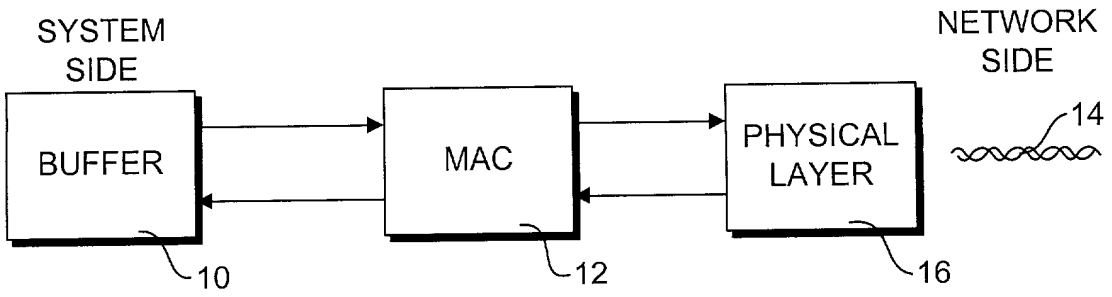


FIG. 1

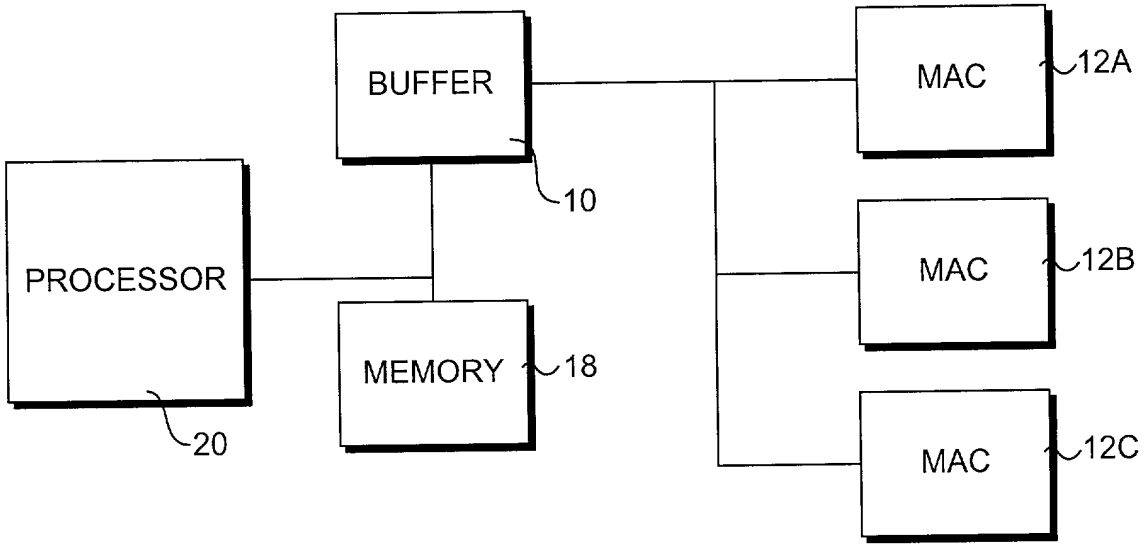


FIG. 2

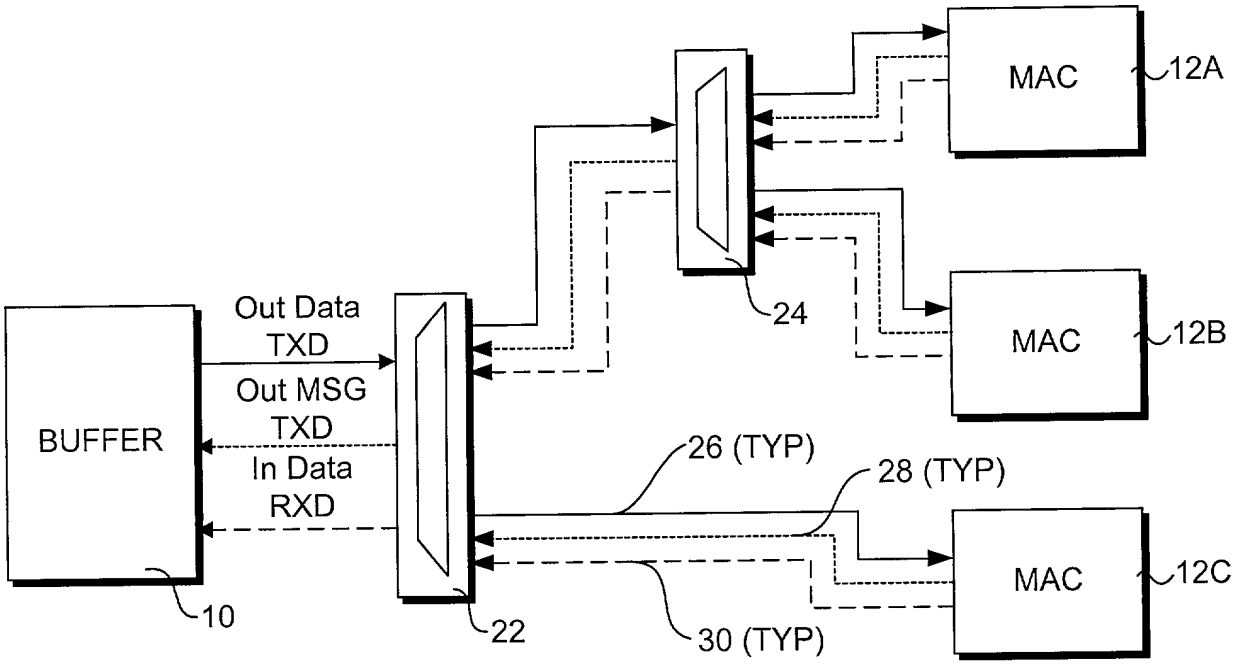


FIG. 3

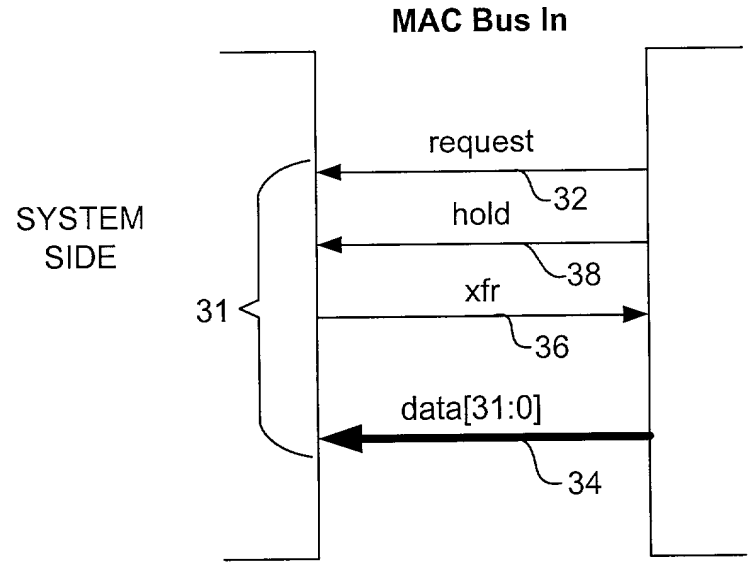


FIG. 4

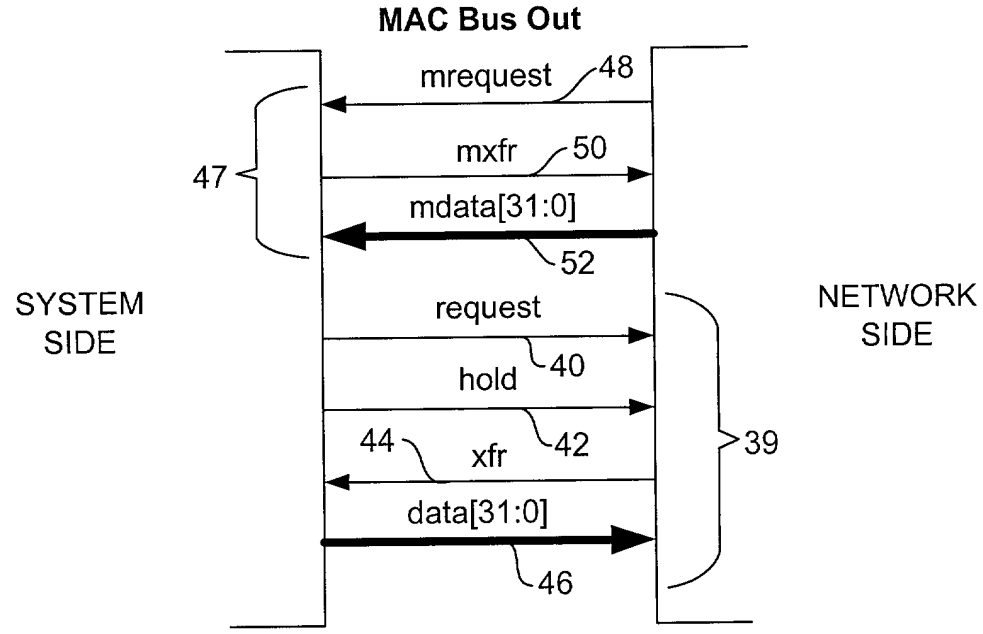


FIG. 5

DATA PACKET HEADER WORD

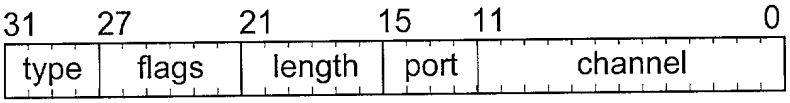


FIG. 6

REQUEST MESSAGE WORD

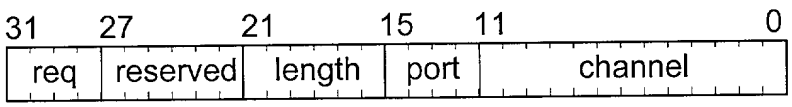


FIG. 7

FIG. 8

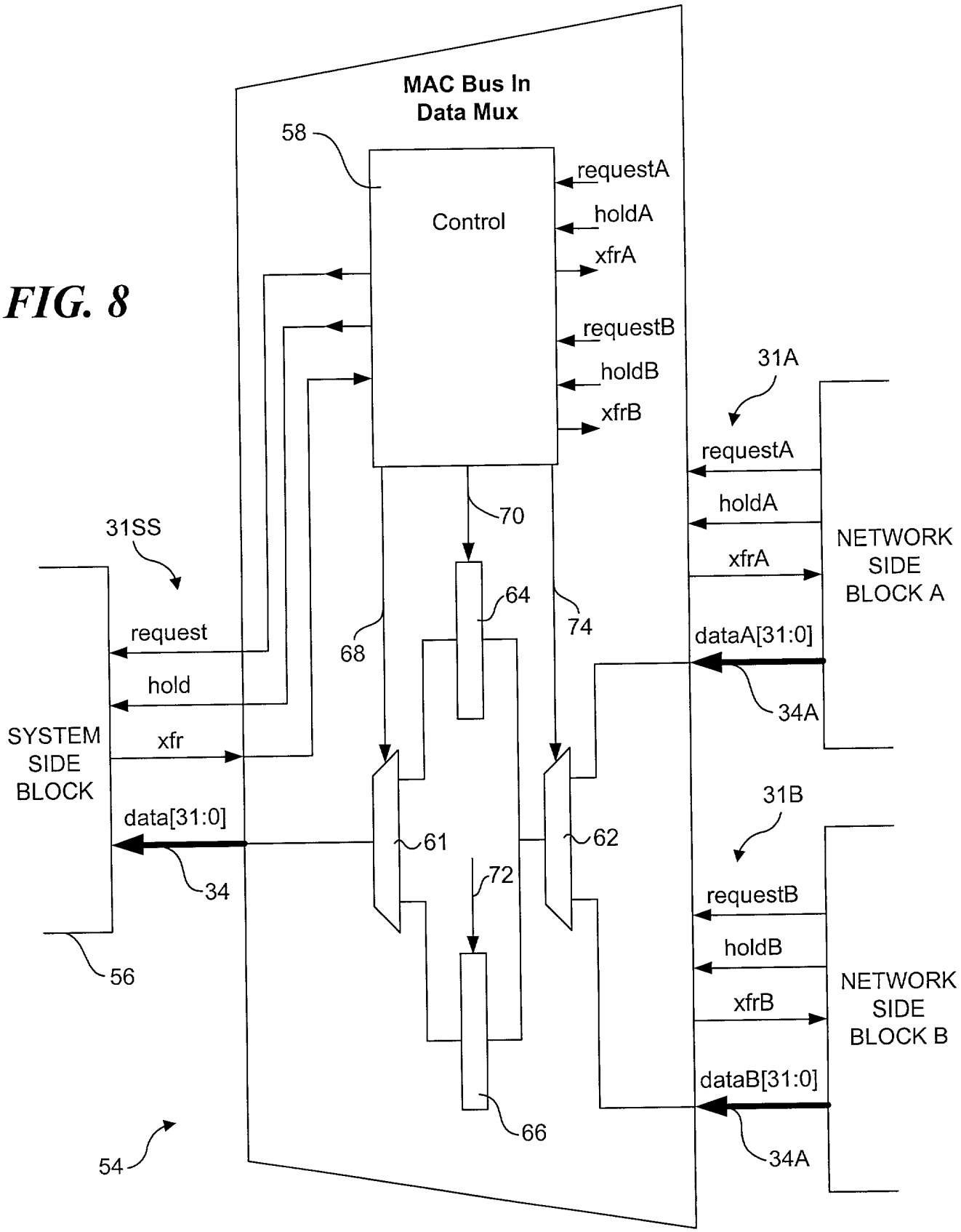
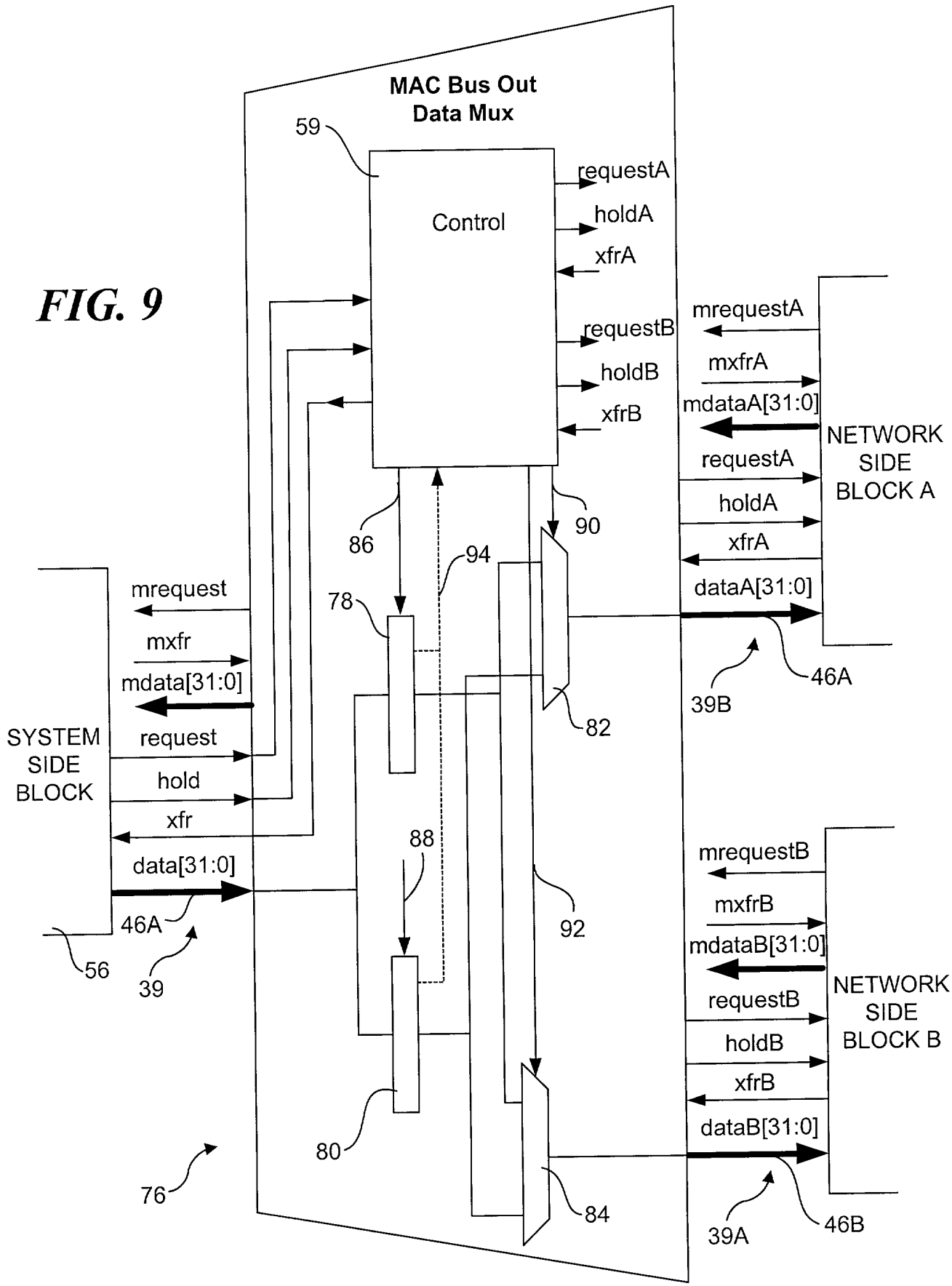

MAC Bus In
Data Mux
58
Control
requestA
holdA
xfrA
requestB
holdB
xfrB
31A
requestA
holdA
xfrA
NETWORK
SIDE
BLOCK A
dataA[31:0]
34A
31SS
request
hold
xfr
SYSTEM
SIDE
BLOCK
data[31:0]
34
56
70
64
68
74
61
62
72
66
31B
requestB
holdB
xfrB
NETWORK
SIDE
BLOCK B
dataB[31:0]
34A
54

FIG. 9


MAC Bus Out
Data Mux
59
Control
requestA
holdA
xfrA
requestB
holdB
xfrB
mrequestA
mxfrA
mdataA[31:0]
requestA
holdA
xfrA
dataA[31:0]
NETWORK
SIDE
BLOCK A
mrequestB
mxfrB
mdataB[31:0]
requestB
holdB
xfrB
dataB[31:0]
NETWORK
SIDE
BLOCK B
mrequest
mxfr
mdata[31:0]
request
hold
xfr
data[31:0]
SYSTEM
SIDE
BLOCK
86
90
94
78
82
88
92
80
84
76
46A
39B
46A
56
39
39A
46B

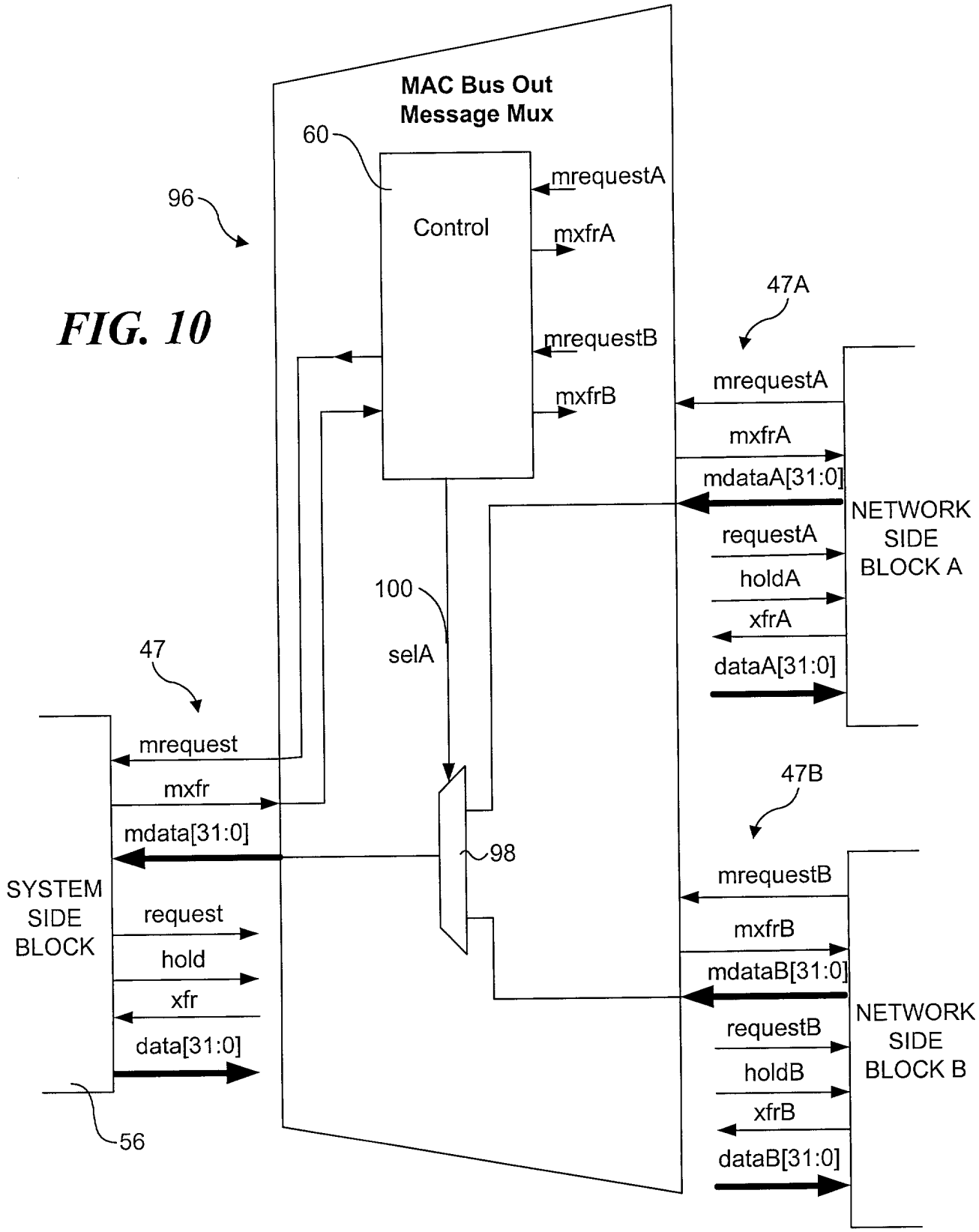

MAC Bus Out
Message Mux
60
Control
96
mrequestA
mxfrA
mrequestB
mxfrB
47A
mrequestA
mxfrA
mdataA[31:0]
NETWORK
SIDE
BLOCK A
requestA
holdA
xfrA
dataA[31:0]
100
selA
47
mrequest
mxfr
mdata[31:0]
98
47B
mrequestB
mxfrB
mdataB[31:0]
SYSTEM
SIDE
BLOCK
request
hold
xfr
data[31:0]
NETWORK
SIDE
BLOCK B
requestB
holdB
xfrB
dataB[31:0]
56

FIG. 10

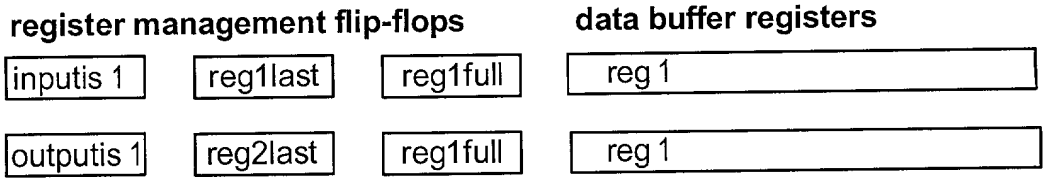


FIG. 11

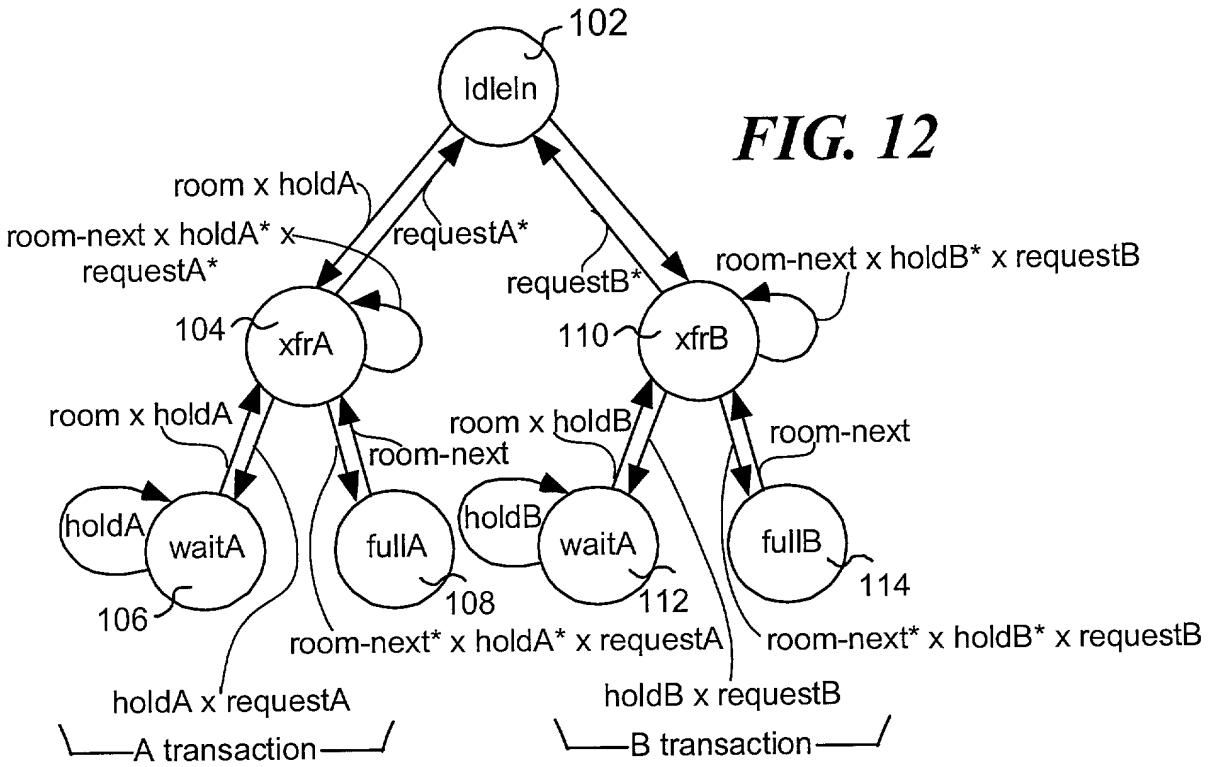
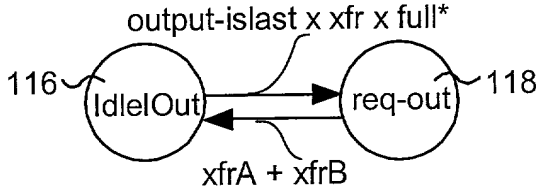


FIG. 12

transaction = IdleIn*
room-next = empty + xfr
room = reg1full* + reg2full + xfr
full = reg1full x reg2full
empty = reg1full* x reg2full*

FIG. 13



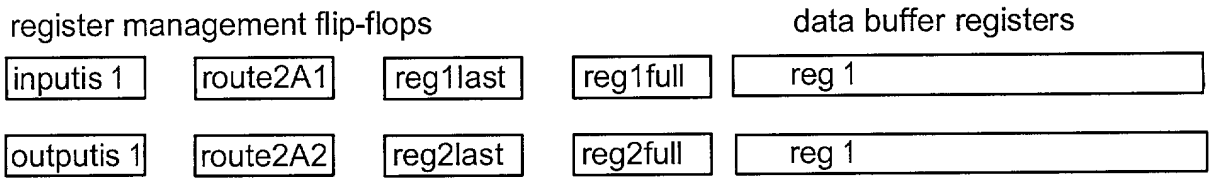


FIG. 14

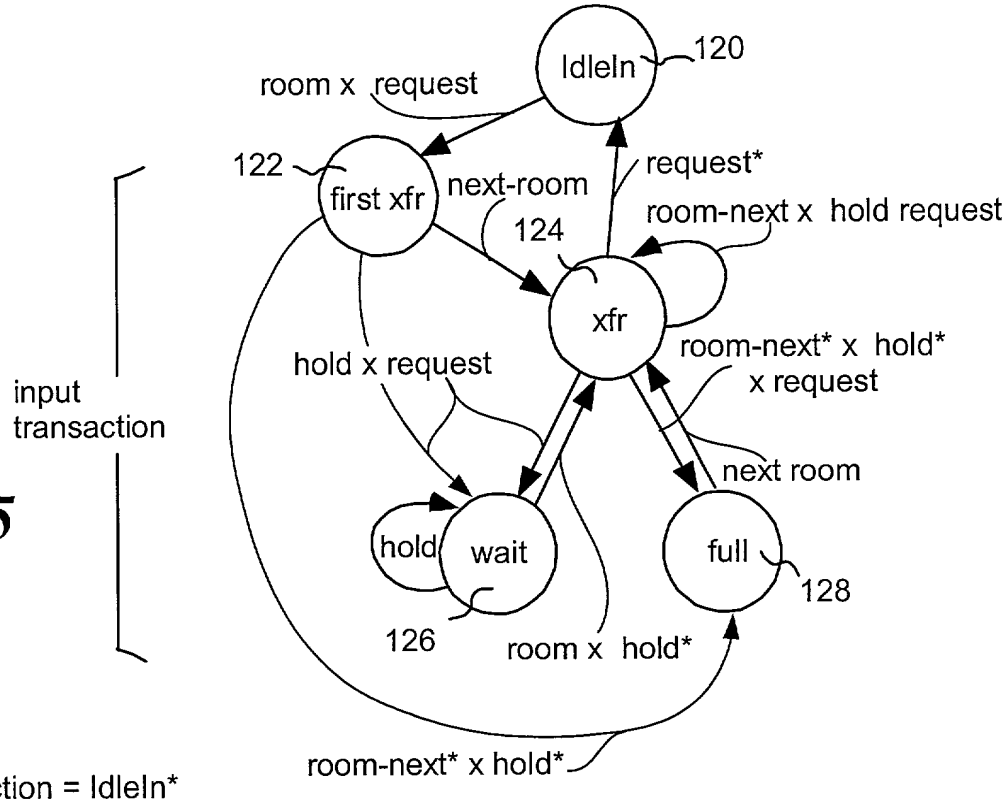


FIG. 15

transaction = IdleIn*
room-next = empty + xfrA + xfrB
room = reg1full* + reg2full* + xfrA + xfrB
full = reg1full x reg2full
empty = reg1full* x reg2full*

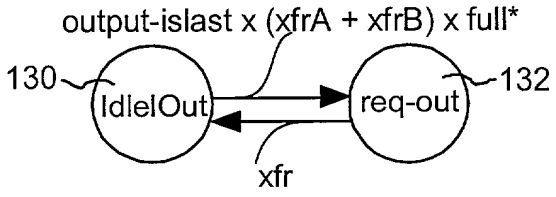


FIG. 16

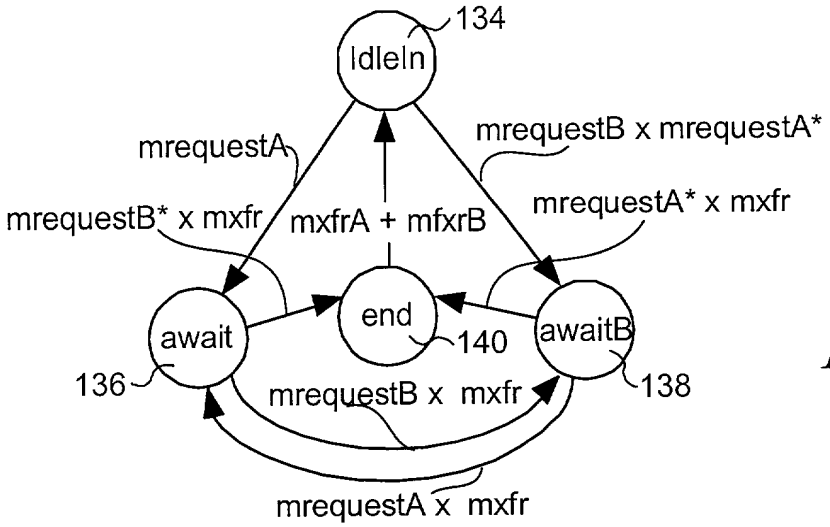


FIG. 17

Message transfers are one word long

merquest = awaitA = awaitB

selA = awaitA

mxfr machines for A and B network side input port

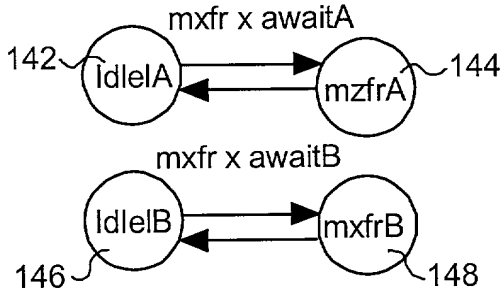


FIG. 18

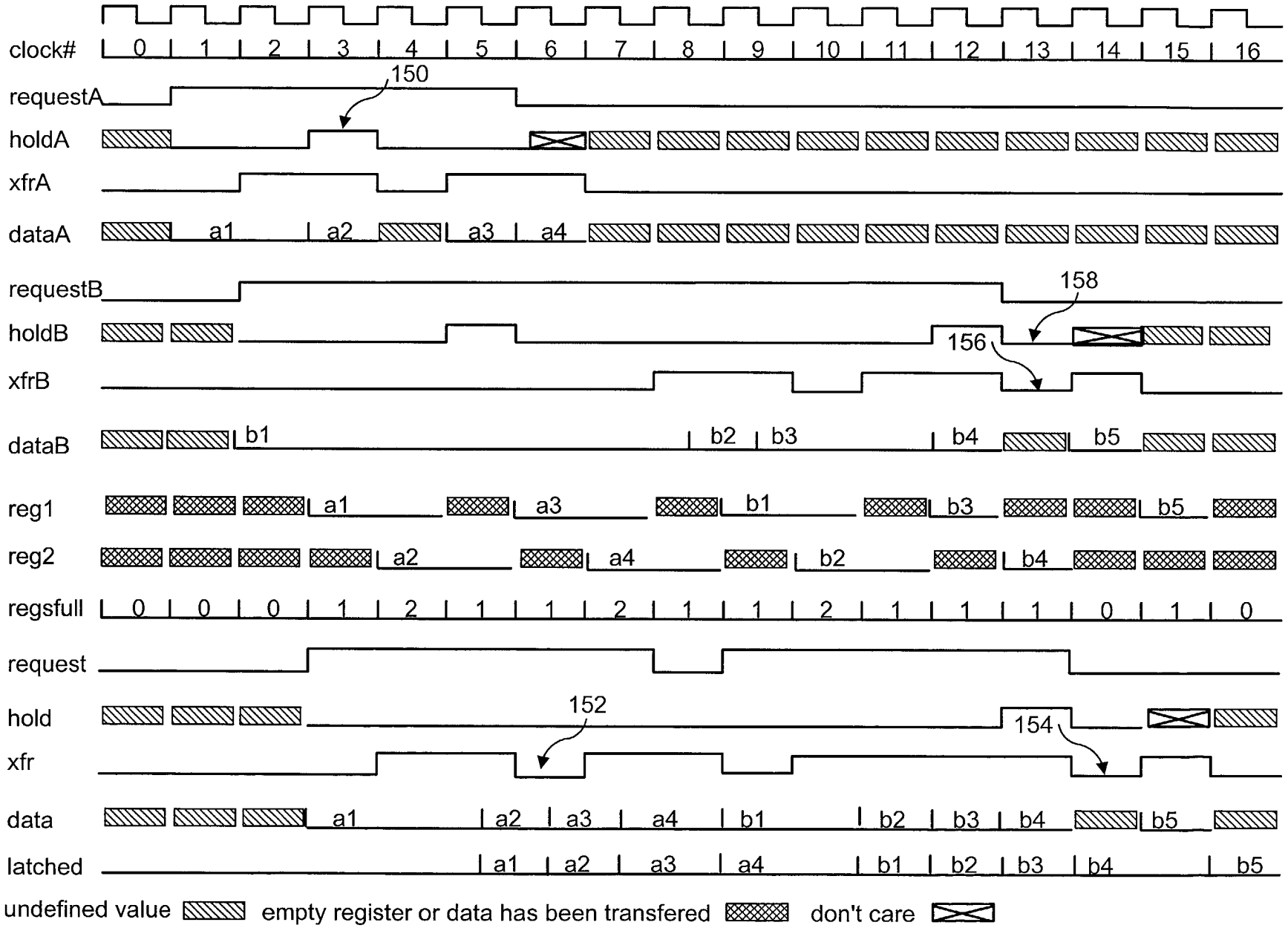

clock#
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
requestA
150
holdA
xfrA
dataA
a1
a2
a3
a4
requestB
158
holdB
156
xfrB
dataB
b1
b2
b3
b4
b5
reg1
a1
a3
b1
b3
b5
reg2
a2
a4
b2
b4
regsfull
0 0 0 1 2 1 1 2 1 1 2 1 1 1 0 1 0
request
hold
152
154
xfr
data
a1
a2
a3
a4
b1
b2
b3
b4
b5
latched
a1
a2
a3
a4
b1
b2
b3
b4
b5
undefined value
empty register or data has been transfered
don't care

FIG. 19

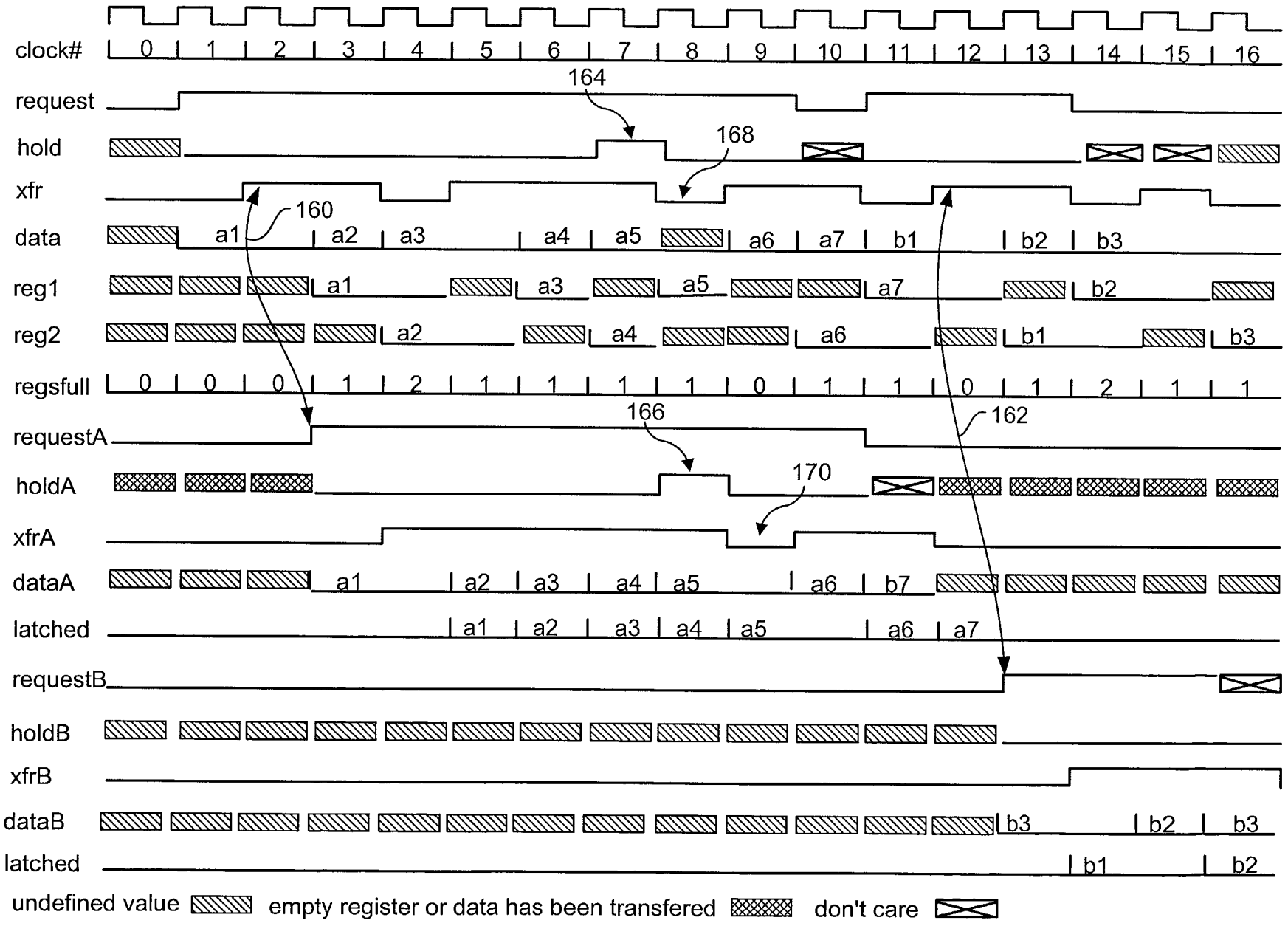

clock#
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
request
164
hold
168
xfr
160
data
a1 a2 a3 a4 a5 a6 a7 b1 b2 b3
reg1
a1 a3 a5 a7 b2
reg2
a2 a4 a6 b1 b3
regsfull
0 0 0 1 2 1 1 1 1 0 1 1 0 1 2 1 1
requestA
166
162
holdA
170
xfrA
dataA
a1 a2 a3 a4 a5 a6 b7
latched
a1 a2 a3 a4 a5 a6 a7
requestB
holdB
xfrB
dataB
b3 b2 b3
latched
b1 b2
undefined value
empty register or data has been transfered
don't care

FIG. 20

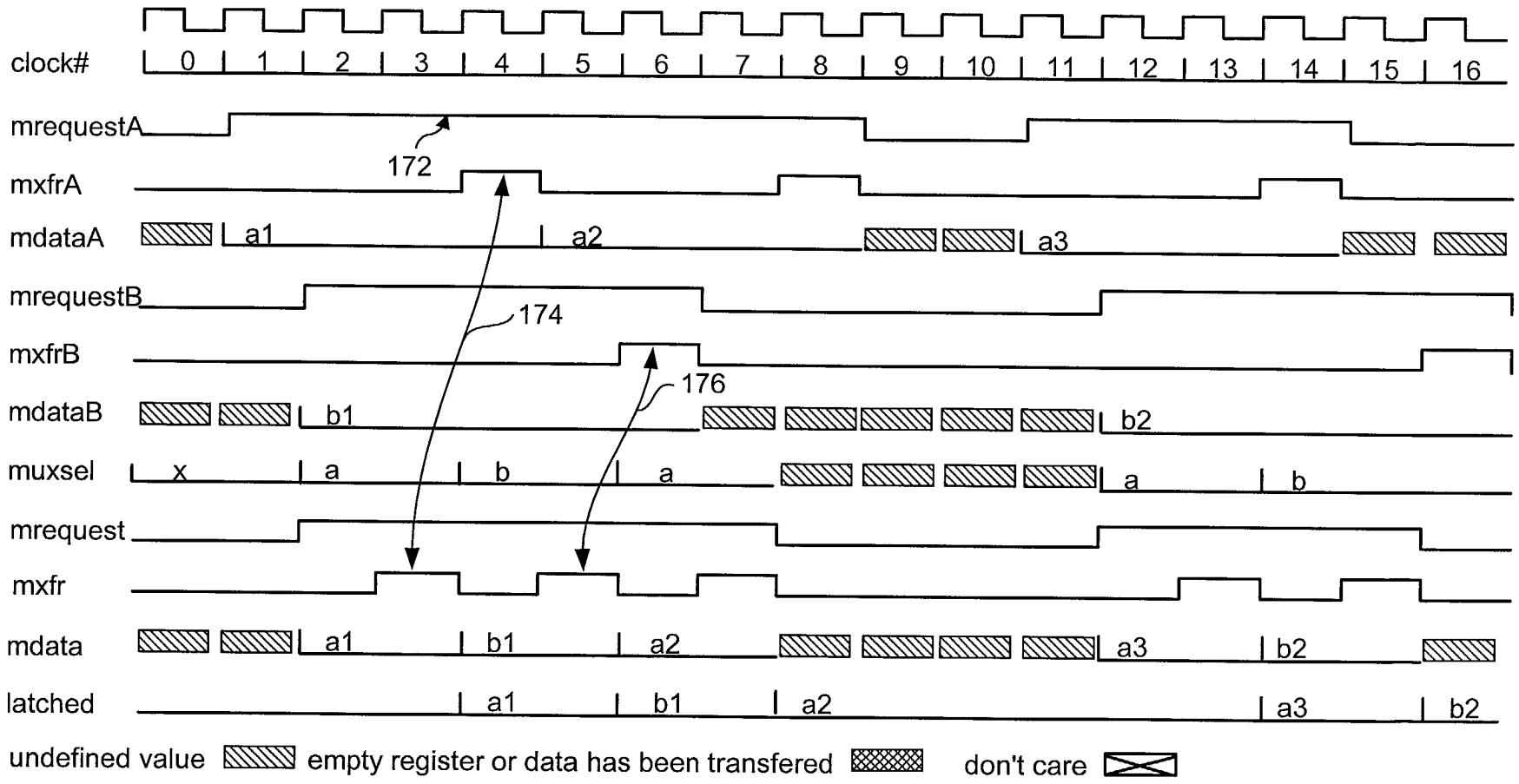

clock#
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
mrequestA
172
mxfrA
mdataA
a1
a2
a3
mrequestB
174
mxfrB
176
mdataB
b1
b2
muxsel
x
a
b
a
a
b
mrequest
mxfr
mdata
a1
b1
a2
a3
b2
latched
a1
b1
a2
a3
b2
undefined value
empty register or data has been transfered
don't care

FIG. 21